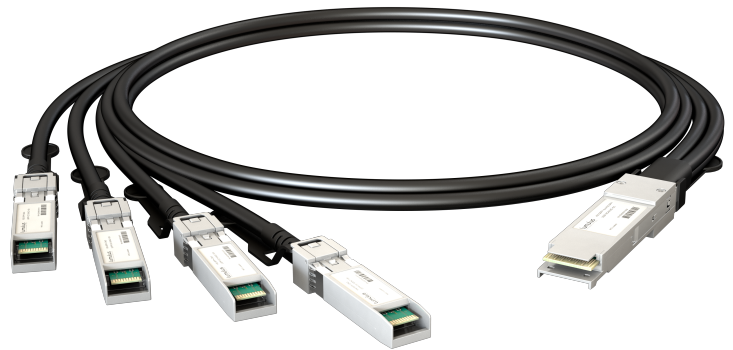


Direct Attach Copper (DAC) Cable

40G QSFP+ to 4x10G SFP+

SFP+



Key Features

- Support 4x10.3125G NRZ
- Single Wire Size: 26AWG~30AWG
- Maximum power consumption:<0.05W each end
- Case temperature range: 0°C to 70°C
- 3.3V Power Supply
- Hot Pluggable
- BER < 10⁻¹⁵
- RoHS Compliance

Applications

- Data center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers



Supported Standards

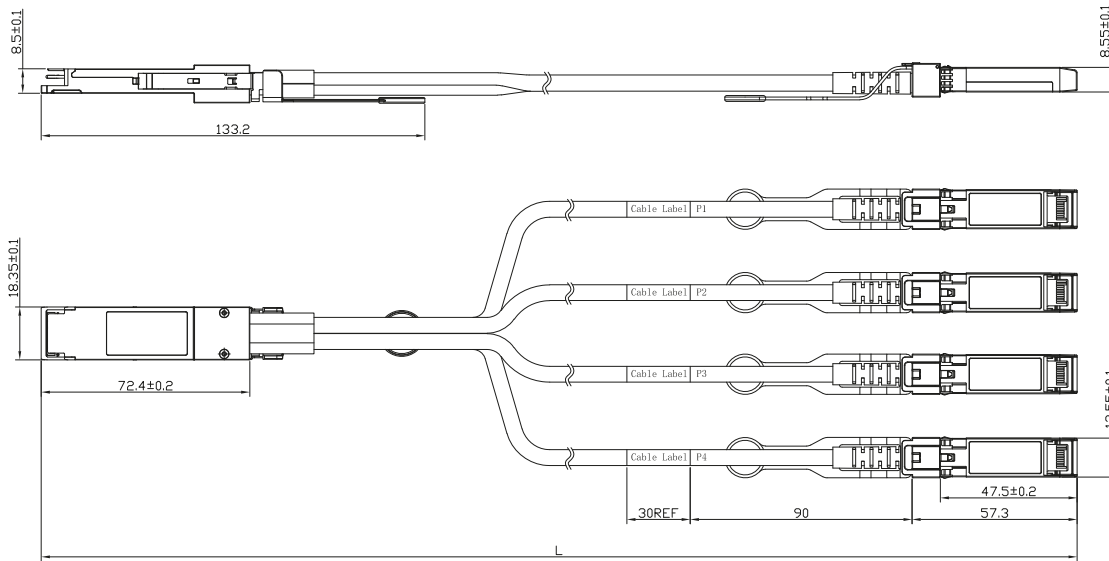
- QSFP+/SFP+ MSA
- SFP+ MSA
- IEEE 802.3ba

Ordering Information

LEQP-WC4xxxC		40G QSFP+ to 4x10G SFP+ DAC (1m~7m)			
Ordering P/Ns	Description	Length	AWG	Cable	
LEQP-WC4010C	40G QSFP+ to 4x10G SFP+ DAC	1m	30AWG	PVC Black	
LEQP-WC4035C	40G QSFP+ to 4x10G SFP+ DAC	3.5m	28AWG	PVC Black	
LEQP-WC4050C	40G QSFP+ to 4x10G SFP+ DAC	5m	24AWG	PVC Black	
LEQP-WC4070C	40G QSFP+ to 4x10G SFP+ DAC	7m	24AWG	PVC Black	

xxx define DAC cable length

Mechanical Outline



40G QSFP+ TO 4*10G SFP+ ACC

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min.	Typ.	Max.	Notes
Supply Voltage	Vcc	V	-0.4	-	+3.6	
Storage Temperature	TS	°C	-40	-	85	
Operating Case temperature	TOP	°C	0	-	70	
Operating Humidity	RH	%	5	-	85	

Recommended Operating Conditions

Parameter	Unit	Min.	Typ.	Max.	Notes
Operating Case Temperature	°C	0		70	
Supply Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		40		

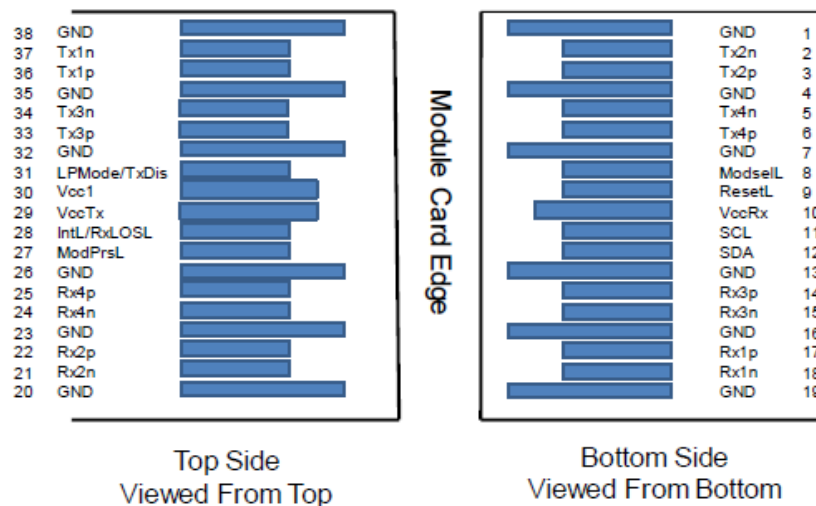
QSFP+ PIN Function Definitions

Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		Vcc Rx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output

25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTTL-O	ModPrsL	Present
28	LVTTTL-O	IntL/RxLOSL	Interrupt/optional RxLOS
29		Vcc Tx	+3.3 V Power supply transmitter
30		Vcc1	+3.3 V Power Supply
31	LVTTTL-I	LPMoDe/TxDis	Low Power Mode/optional TX Disable
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground

QSFP+ Transceiver Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP56 MSA.



SFP+ PIN Function Definitions

Pin	Logic	Symbol	Description
1		VeeT	Module Transmitter Ground
2	LVTTL-O	Tx_Fault	Module Transmitter Fault
3	LVTTL-I	Tx_DIS	Transmitter Disable; Active High Disable Transmitter Output
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data
5	LVTTL-I/O	SCL	2-Wire Serial Interface Clock
6		Mod_ABS	Module Absent, connected to VeeT or VeeR in the module
7	LVTTL-I	RS0	Rate Select0, optionally controls SFP+ module receiver
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication
9	LVTTL-I	RS1	Rate Select1, optionally controls SFP+ module transmitter
10		VeeR	Module Receiver Ground
11		VeeR	Module Receiver Ground
12	CML-O	RD-	Receiver Inverted Data Output
13	CML-O	RD+	Receiver Non-Inverted Data Output
14		VeeR	Module Receiver Ground
15		VccR	Module Receiver 3.3V Supply
16		VccT	Module Transmitter 3.3V Supply
17		VeeT	Module Transmitter Ground
18	CML-I	TD+	Transmitter Non-Inverted Data Input
19	CML-I	TD-	Transmitter Inverted Data Input
20		VeeT	Module Transmitter Ground

SFP+ Electrical Pad Layout

